

Soft-Core Dataflow Processor Architecture Optimised for Radar Signal Processing

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Abstract

Current radar signal processors lack either performance or flexibility. Custom soft-core processors exhibit potential in high-performance signal processing applications, yet remain relatively unexplored in research literature. In this paper, we use an iterative design methodology to propose a novel softcore streaming processor architecture. The datapaths of this architecture are arranged in a circular pattern, with multiple operands simultaneously flowing between switching multiplexers and functional units each cycle. By explicitly specifying instruction level parallelism and software pipelining, applications can fully exploit the available computational resources. The proposed architecture exceeds the clock cycle performance of a commercial high-end DSP processor by an average factor of 14 over a range of typical operating parameters in a radar signal processor application.